Parasitic-Aware Design and Optimization of CMOS RF Integrated Circuits

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Abstract

The need for higher integration and lower cost personal communication systems (PCS) has motivated extensive efforts to develop CMOS RF integrated circuits which meet the performance requirements of current and future standards such as IS-95, GSM, DECT, etc. However, power losses associated with on-chip inductor, device, and package parasitics have impeded the full integration of power-efficient CMOS RF ICs. In this paper, we describe a custom CAD synthesis and optimization tool which enables RF chip/package design for optimum circuit performance. A fully-integrated CMOS power amplifier (PA) illustrates the efficacy of this approach.

Introduction

In order to achieve low-cost integrated circuits for PCS, key RF circuit blocks such as power amplifiers, low noise amplifiers (LNAs), up- and down-conversion mixers, transmit switches, etc., must be fully integrated. Complete integration of one-chip transceivers with both digital baseband and analog RF functions dictates the use of low-cost sub-micron digital CMOS technology [1]-[4]. A common characteristic of many previously reported RF CMOS circuits is the use of off-chip passive networks; they often use RF chokes, inductors, bond wires, etc., to "tune" circuit responses for improved performance such as low LNA noise figures, high PA power efficiencies, etc. Off-chip elements increase cost and reduce long-term reliability, but their use has been mandated by the lack of chip/package design tools to facilitate synthesis and optimization of RF circuits.

While manually adjusting off-chip tuning networks leads to high-performance designs, those costs can be eliminated by including parasitics as an integral part of the design process. This is not a trivial matter. For example, a simple two-element LC matching section is easily synthesized using a Smith chart. However, if all parasitic elements associated with lossy on-chip capacitors and inductors implemented in a digital CMOS process are included, the Smith chart approach quickly becomes unwieldy. In this paper, we describe a custom CAD tool that enables package/chip co-synthesis and optimization of fully-monolithic RF circuits. This tool is based on the well known simulated annealing algorithm [5] and works to optimize RF circuit performance in the presence of known device, package, and passive element parasitics.

Parametric Modeling of Planar Inductors

We begin by considering the parametric inductor models which are essential to computer-aided synthesis and optimization approaches. Inductors fabricated on silicon suffer resistive losses due to the substrate and the metal layer(s) used to form the inductor. Substrate losses are caused by both inductive and capacitive coupling between the inductor metal layer(s) and the substrate. The flux generated in the coil links the substrate and induces eddy currents in it. These eddy currents flow in opposition to the inductor current and give rise to a negative coefficient of mutual inductance between the inductor and the substrate. Even in the case of a heavily-doped substrate, however, the substrate resistivity is usually much larger than that of the metal(s) forming the inductor. Thus, the effects of substrate eddy currents on the inductance are negligible, but their effects on inductor losses are significant and must be considered. Capacitive coupling occurs due to the SiO_2 between the inductor metal layer(s) and the substrate. Parasitic-aware optimization requires parametric models in which all desired and parasitic element values are expressed in terms of L and C values over ranges of interest.

To obtain a parametric planar inductor model, we have adopted an approach similar to [6]-[7]. The on-chip inductor is first segmented, and each segment is modeled by a lumped equivalent circuit including a self-inductance, a series resistance equal to the dc resistance of the metal segment, a shunt capacitance representing the capacitive coupling between the metal forming the segment and the substrate, an effective substrate loss resistance computed simply as a lateral spreading resistance [8], and an inter-turn coupling capacitance. Positive and negative mutual inductance terms between segments on opposite sides are also included. The effects of corners (or bends) are neglected and assumed to be insignificant at our 1GHz frequencies of interest. Figure 1 shows a five segment planar inductor and

* Supported by the National Science Foundation Center for the design of Analog/Digital Integrated Circuits (CDADIC) and by research grants from the Hewlett-Packard Company and Texas Instruments, Inc.

its lumped model. Although very accurate, that model is not suitable for CAD because the simulated annealing algorithm requires tens of thousands of iterations to reach an optimum solution. Hence, use of the complex circuit model of Figure 1(b) for every inductor is prohibitive in terms of computation time. To iteratively optimize a circuit over a range of inductances requires a reasonably accurate but much more compact model of the inductor. Over the frequency range of interest (not all frequencies), the compact circuit model of Figure 2 is used to approximate the impedance versus frequency behavior of the complex model of Figure 1(b). The L value is obtained using Greenhouse's method [6]. R_s is the total dc series resistance of all metal segments forming the inductor. C_1 and R_1 are chosen so that the compact model has the same Q and f_{max} as the inductor or its complex model:

$$Q = \frac{1}{R_1 + R_s} \cdot \sqrt{\frac{L}{C_1}} \quad (1)$$

$$f_{max} = \frac{1}{2\pi\sqrt{LC_1}} \quad (2)$$

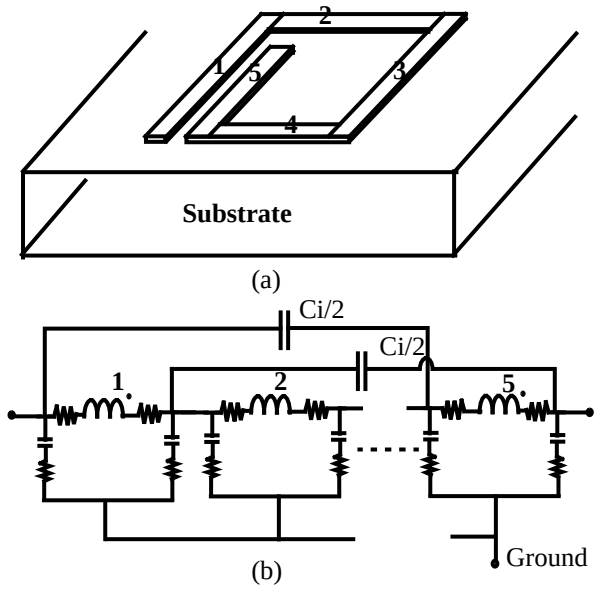

Figure 1. (a) A five segment inductor and (b) the complete equivalent circuit used to model it.

By repeating this procedure for a set of inductors, R_s, R_1, and C_1 are obtained for L values over a desired range of interest. Polynomials are used to parameterize the parasitic values as a function of L. For the process and design parameters listed in Table 1, the following parametric equations were obtained for a floating inductor in the range of 1nH to 18nH

$$R_s = -0.0278L^2 + 1.741L + 2.3402 \quad (3)$$

$$C_1 = -0.0005L^2 + 0.0307L + 0.0468 \quad (4)$$

$$R_1 = -0.0894L + 32.151 + 3.5064/L \quad (5)$$

where L is in nH, C_1 is in pF, and R_1 and R_s are in ohms. Parasitic values for any inductance value, in the given range, can be estimated using these parametric equations. Note that these equations are specific to the geometry of the inductor, and to the configuration in which the inductor is used; i.e., floating or with one end grounded. Figure 3 compares the simulation results for the impedance versus frequency of a 7.8nH, 23 segment inductor with the circuit resulting from equations (3)-(5). Excellent agreement is observed between the two cases up to the first-resonant frequency. This set of parametric equations is incorporated into the CAD tool for predicting inductor parasitics.

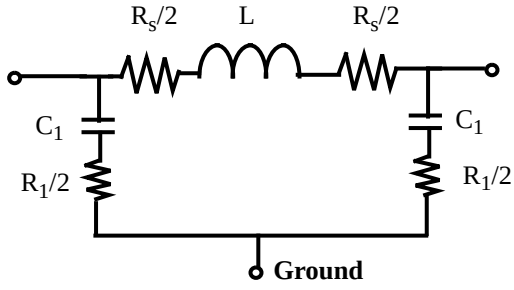

Figure 2. Compact model for the inductor.

Table I: CMOS Process and Inductor Geometry Parameters.

Parameter	Value
Sheet resistance of metal3	0.05 ohm/sq
Metal3 capacitance to substrate	20aF/μm^2
ε_{ox}	4
Length of shortest segment	100μm
Width of metal3 segments	15μm
Edge-edge spacing between turns	1.2μm

Simulated Annealing/CAD Optimization

Simulated annealing is a heuristic which can be used to iteratively arrive at a solution to a problem while minimizing some error function. Although simulated annealing is not guaranteed to arrive at the best solution every time, as the number of iterations increases, the probability of arriving at the best solution approaches unity [5]. This algorithm is based on the metallurgical process of annealing. Similar to its mechanical counterpart, the "temperature" of the solution to the problem is gradually reduced and at lower temperatures the system approaches the optimum solution (analogous to a highly ordered state in the mechanical process of annealing solids). This algorithm has the advantage that the probability of getting trapped in a local minima is low since

at higher temperatures, the solution has a high enough probability of accepting a worse solution than the accepted solution, and thus jump out of a local minimum. As the temperature is reduced, and if enough iterations are carried out at each temperature, the annealer finds the global minimum. Practical design experience indicates that there is more than one set of values for the elements of a matching network being used to tune an RF circuit which results in acceptable performance. Simulated annealing is ideally suited to find the global minimum in the presence of such local minima.

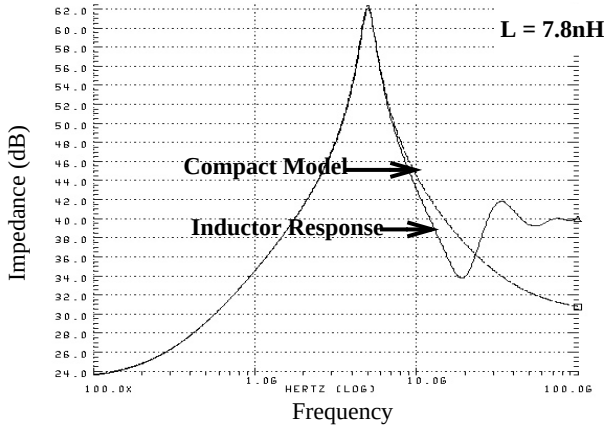

Figure 3. Inductor and compact model response.

While this CAD tool has been used to design matching networks with lossy inductors (it took 10mS system time on a HP712/80MHz machine to design an L-section to transform 50ohm to 19.86 + j6.04 ohm with the goal being 20 + j6 ohm), it is more beneficial to directly optimize the circuit/package being designed. In such case, it could be used to determine the optimum pin configuration for a given package, as well as the design of any integrated passive networks. As an example, this CAD tool has been implemented to optimize the efficiency of a power amplifier implemented in CMOS technology, and with an integrated output matching network. Figure 4 shows the flow-chart for this CAD tool. A certain number of iterations are carried out at each temperature (an abstract measure of the probability of accepting a solution worse than the presently accepted solution). Each iteration involves selecting a solution set (which may consist of values for the various passive elements, as well as package parasitic values corresponding to specific pins of the package) and evaluating the cost, or error, function. This function can be efficiency in the case of PAs, or gain/noise figure in the case of LNAs. The solution is accepted if it is better than the previously accepted solution, and conditionally accepted otherwise. This process is repeated for different temperature values until either a certain number of iterations are performed or the goal is met.

This CAD tool was used to optimize the PA circuit shown in Figure 5. The PA has been designed to supply 100mW into a 50 ohm load, at 900MHz, and works from a single 3V supply. The circuit was optimized for efficiency by changing the topology as well as the value of the elements forming the matching network. Matching network topologies tried out included two L-sections, a pi section, and a simple inductor. Before optimization, the PA exhibited a drain efficiency of 36%, using an L-section as an output match. After a few days of optimization, an L-section was found for which the PA had an efficiency of 49%, while a simple inductor used as the matching network achieved an efficiency of 57%. Thus, the use of this CAD tool resulted in a dramatic improvement in the efficiency of the amplifier,

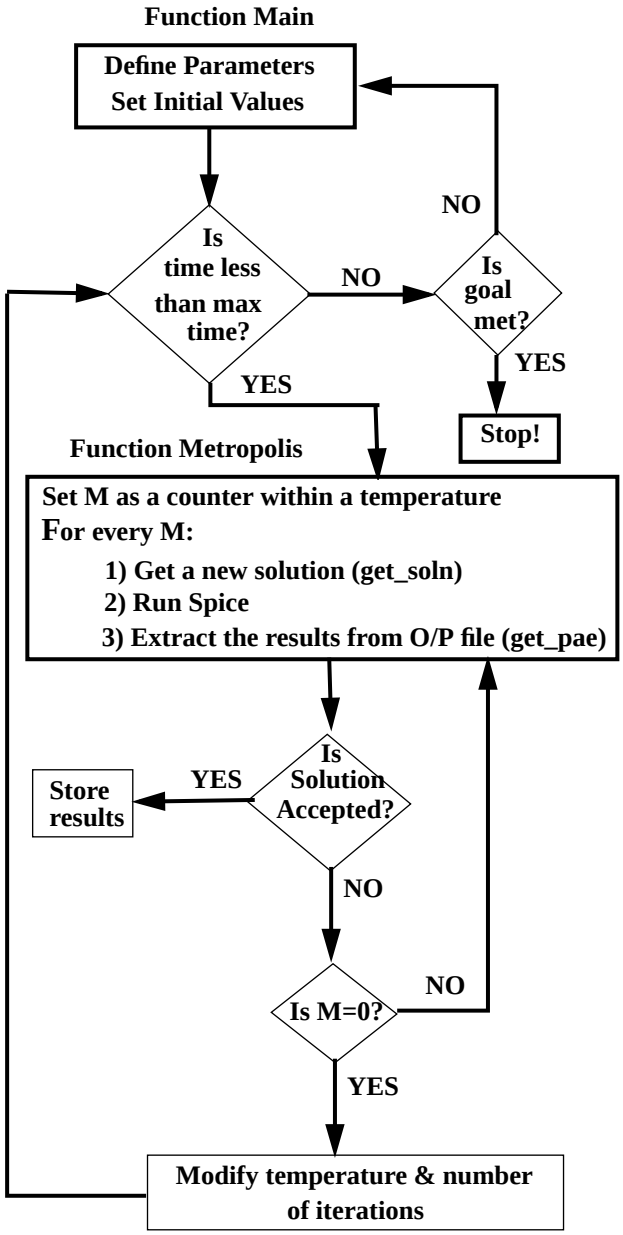

Figure 4. Flow of the simulated annealing CAD tool.

even with the use of high loss inductors in the output matching network. This amplifier has been fabricated in a 0.5µm digital CMOS process, and drain efficiency close to 50% has been measured at an output power of 100mW at 900MHz (see Figure 6). A die photograph of the fully-monolithic CMOS PA is shown in Fig. 7.

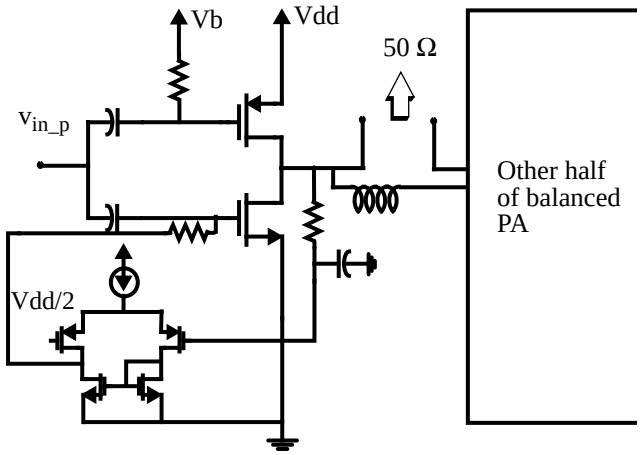

Figure 5. Balanced PA with a PMOS load.

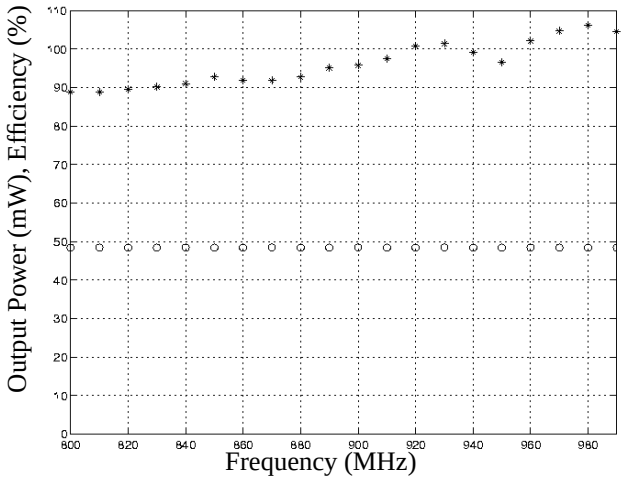

Figure 6. Measured output power(∗) and efficiency(o) versus frequency.

Conclusions

We have demonstrated the benefits to be gained from optimization of RF circuits designed considering chip and package parasitics as an integral part of the design process. A simulated annealing based CAD tool has been developed to achieve a significant improvement in the performance of a power amplifier implemented in digital CMOS technology. In order to implement fully monolithic RF circuits, parasitic-aware design and optimization needs to be an integral part of the chip/package design process.

Acknowledgments

The authors thank Motorola, Inc. for supporting R. Gupta as a Ph.D. intern, and specifically J. Rollman and C. Griffin for measurement assistance, and M. Green for wire bonding. Many helpful discussions with Ed Godshalk of Maxim Integrated Products and Dr. Stewart S. Taylor of Triquint Semiconductor are acknowledged as is the assistance of Ramsin Ziazadeh of Oregon State University in developing the code for the simulated annealing CAD tool.

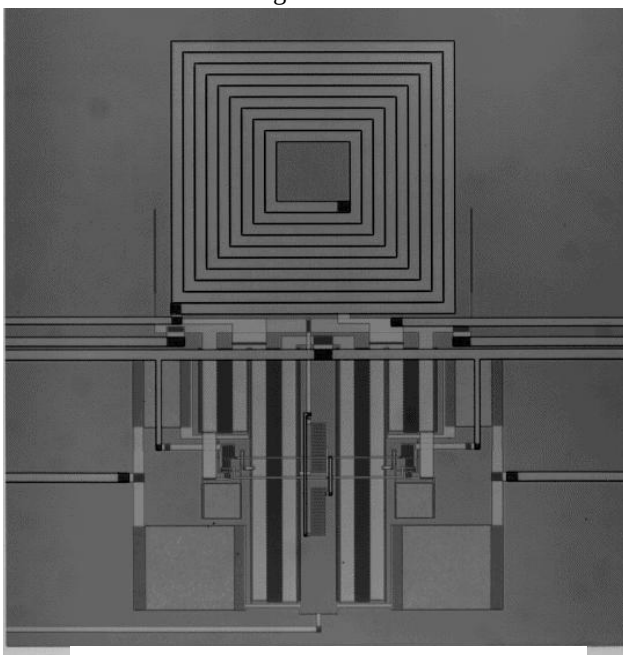

Figure 7. Die photograph of the balanced PA including the metal3 on-chip spiral inductor.

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